IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Andrew MacCormack et al.
Application No.	:	09/239,907
Filed	:	January 29, 1999
For	:	DIGITAL RECEIVER DEMULTIPLEXER
Examiner	:	Scott E. Beliveau
Art Unit	:	2623
Docket No.	:	858063.435
Date	:	December 17, 2007

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' REPLY BRIEF

Commissioner for Patents:

This reply brief is in furtherance of the Notice of Appeal, filed in this case on June 8, 2006, and is in response to the Examiner's Answer mailed October 17, 2007. Appellants hereby request any fees necessary for acceptance of this Reply Brief be charged to Deposit Account No. 19-1090.

I. ARGUMENT IN REPLY

Although the Examiner has rejected each of claims 1, 3-11, 13-42, 45, and 46 under either 35 U.S.C. §§ 102, 103, or 112, Final Office Action, the Examiner has not made out a *prima facie* case on any of the grounds for rejection. Essentially, most of the Examiner's rejections are based on interpretations of snippets from the claims in a vacuum, rather than in the context of the claims and the specification. Each ground of rejection will be addressed in turn.

A. *Claims 1 and 3-10 Are Enabled and Comply With the Written Description Requirement*

The thrust of the Examiner's argument is that the specification makes it clear that a match signal is set by the third control circuit rather than by the input module. On this point, the Examiner and Applicants agree, at least with respect to the embodiments claimed in claims 1 and 3-10. Thus, the Examiner's Answer further supports Appellants' position that the Examiner's interpretation of claims 1 and 3-10 as requiring that the input module sets the match signal is an unreasonable misreading of the claims.

The Examiner relies on proximity instead of context to define the scope of claims 1 and 3-10. The last paragraphs of claims 1 and 10 recite "a ***third control circuit*** for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, ***for setting a match signal*** to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the ***second control circuit*** accesses the address in the memory to retrieve control information associated with the packet identifier and ***controls processing*** of the input data packet responsive to the match signal ***by the input module***." Despite acknowledging that claims 1 and 3-10 expressly recite that the third control circuit sets the match signal, the Examiner points to the phase "match signal by the input module" out of context to incorrectly assert that claims 1 and 3-10 also require that the match signal be set by the input module. The Examiner inserts the words "be set" between "match signal" and "by the input module" and ignores the phrase "control processing of" Claims 1 and 10 (emphasis added). Claims 1 and 3-10, however, do not recite "match signal ***set by*** the input module." When the last clause is considered as a whole, and thus in context, claims 1 and 3-10 make it clear that the third control circuit sets the match signal, and do not also recite or even suggest that the match signal ***is set*** by the input module. The claims are not even arguably ambiguous on this point. Accordingly, the Examiner has not established a *prima facie* case of non-enablement or lack of written description, and thus, the Section 112 rejections of claims 1 and 3-10 should be reversed.

B. *Claims 39-41 Are Not Anticipated by Dokic*

Independent claim 39 recites "a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory, wherein responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information." The Examiner argues without explanation that the claims do not limit "associated control information." The Examiner has not rejected claims 39-41 as indefinite, and the burden of proof is on the Examiner, not the Applicants. The Examiner also is again incorrectly interpreting a phrase by ignoring the context of the claims.

The Examiner identifies the host processor 106 as the claimed receiver processor and first points to the PID filtering table as both the "desired packet identifiers" and as the "associated control information." The desired packet identifiers and the associated control information are separately recited as stored by the receiver processor in claim 39. Claim 39 does not read "desired packet identifiers ***comprising*** associated control information," it reads "desired packet identifiers ***and*** associated control information." Further, there is no indication that the PID filtering table of Dokic in fact comprises stored associated control information. The Examiner has not met his burden of proof, as explained in Appellants' opening brief.

In the Answer, the Examiner next points to column 6, lines 1-5 and column 13, lines 63-65, and argues that the host processor stores default PIDs, and this somehow equates to storing desired packet identifiers and associated control information. As explained in Applicants' opening brief, in Dokic default PIDs are recovered from the transport stream when a PID filtering table is not available. Thus, even assuming, *arguendo*, that default PIDs constitute "desired packet identifiers" and "associated control information" (they do not), there is no indication in Dokic that control information is retrieved "responsive to a match," as recited.

Accordingly, the Examiner has not meet his burden of establishing a *prima facie* case of anticipation, and the Examiner's rejection of claims 39-41 should be reversed.

C. *Claims 45 and 46 Are Not Anticipated by Dokic*

The Examiner in the Answer argues that storing the type of data packet or information used by a clock recovery system would satisfy the limitation "means for retrieving control information associated with a received data packet." The Examiner, however, has not established that Dokic stores the type of data packet or the timing information in the memory 205. The portion of Dokic to which the Examiner points (column 8, lines 24-52) does not suggest that the type of data packet or the timing information is stored in (or retrieved from) the memory 205. To the extent the Examiner is referring to the timing information, this information is not stored in the memory 205. Instead, the memory stores the PIDs of packets in the transport stream that contain the timing information.

Accordingly, the Examiner has not meet his burden of establishing a *prima facie* case of anticipation, and the Examiner's rejection of claims 45 and 46 should be reversed.

D. *The Examiner has Failed to Establish a* Prima Facie *Case that Dokic in view of the Manual Renders Claims 11 and 13-20 Obvious.*

The Examiner essentially argues that the data buffers in the data stream may be considered as a memory separate from the data stream because the claims do not prohibit the separate memory from also storing data packets. This argument is a non sequitur and is unreasonable because the specification describes the data stream and separately illustrates and describes the data SRAM 400. One of skill in the art would not interpret data buffers in the data stream as a memory that is separate from the data stream, regardless of whether the separate memory might also sometimes store all or part of a data packet. Accordingly, the Examiner has not meet his burden of establishing a *prima facie* case of obviousness, and the Examiner's rejection of claims 11 and 13-20 should be reversed.

E. *The Examiner has Failed to Establish a* Prima Facie *Case that Dokic in View of Blatter Renders Claims 21-38 Obvious.*

The claims recite two data structures, one which stores addressing information accessed based on packet identifiers and another which stores control information that is accessed based on addressing information extracted from the other data structure.

The Examiner admits that Dokic does not disclose or suggest the claimed first **and** second data structures. The Examiner contends memory 205 of Dokic is a data structure

that stores addressing information which is accessed based on packet identifiers, but the Answer does not explain how or whether the memory 205 satisfies the claim limitations. The Examiner also points to units 45 of Blatter as both data structures. The Examiner does not identify how to combine unit 45 with Dokic so as to achieve the claimed invention. The Examiner instead suggests in a conclusory manner that one would be motivated to do so and that the combination would produce a result similar to the one disclosed by Applicants. This is not the same thing as making a *prima facie* case that the claim limitations are satisfied. Further, one of skill in the art would not be motivated to combine Dokic with Blatter. Dokic is directed to "a decoder having a decoupled hardware architecture for demultiplexing and decoding a digital data stream." Dokic, Column 1, lines 6-9. The Examiner also argues that it would be advantageous to modify Dokic to use the data structures of the Manual, and thus incorrectly concludes that Dokic (which teaches decoupling demultiplexing from decoding) does not teach away from the combination. This argument is a non sequitur, and also constitutes improper hindsight reasoning.

Accordingly, the Examiner has not meet his burden of establishing a *prima facie* case of obviousness, and the Examiner's rejection of claims 21-38 should be reversed.

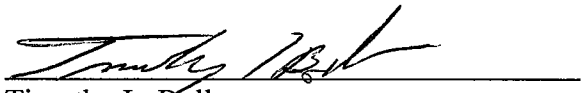
F. *The Examiner has Failed to Establish a* Prima Facie *Case that Dokic in View of Bestler Renders Claim 42 Obvious.*

Claim 42 depends from claim 39. The Examiner does not contend in the Answer that the features of claim 39 that are missing from Dokic, as discussed above, are taught, suggested or motivated by Bestler. Accordingly, Applicants respectfully submit that claim 42 is not rendered obvious by Dokic in view of Bestler and that the Examiner has not established a *prima facie* case of obviousness.

II. CONCLUSION

For at least the reasons set forth in Appellants' opening brief and those set forth above, the Examiner has failed to meet his burden of establishing a *prima facie* case for rejecting the claims. Accordingly, Applicants respectfully submit that all of the pending claims are allowable and request that the Examiner's rejections thereof be reversed.

Respectfully submitted,
Seed Intellectual Property Law Group PLLC



Timothy L. Boller
Registration No. 47,435

TLB:jms

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

1078720_1.DOC